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15CS72

Seventh Semester B.E. Degree Examination, Feb./Mar.2022 Advanced Computer Architectures

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Define computer architecture. Explain Flynn's classification with necessary diagrams. (08 Marks)
- b. With a neat diagram, explain the vector super computer architecture. (08 Marks)

OR

- 2 a. With the necessary diagrams, explain the shared memory multiprocessors. (10 Marks)
- b. What is data dependence? Define all five types of data dependence. (06 Marks)

Module-2

- 3 a. Explain the levels of parallelism in program execution on modern computers. (10 Marks)
- b. What is mode duplication? With an example, explain the node duplication scheduling to eliminate communication delays between processors. (06 Marks)

OR

- 4 a. With diagrams, explain the pipelining in super scalar processors and VLIW processors. (10 Marks)
- b. Explain the memory hierarchy technology. (06 Marks)

Module-3

- 5 a. With a neat diagram, explain backplane bus systems. (06 Marks)
- b. With a neat block diagram, explain the C-access-interleaved memory organization which allows block access in a pipelined fashion. Also sketch the timing chart indicating the major and minor cycle time. (10 Marks)

OR

- 6 a. For the reservation table of a non-linear pipeline shown below:

| | | | | | | |
|----------------|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 |
| S ₁ | X | | | | X | |
| S ₂ | | | X | | | |
| S ₃ | | X | | X | | X |

- (i) Determine the forbidden latency set and initial collision vector.
- (ii) Draw the state transition diagram.
- (iii) List all simple cycles and greedy cycles.
- (iv) Determine MAL. (10 Marks)
- b. Differentiate between CSA and CPA adders. Design a pipeline unit for fixed-point multiplication of 8-bit integers using CSA tree. (06 Marks)

Module-4

- 7 a. Explain the routing in Omega networks of the multiprocessor system. (10 Marks)
- b. Explain the snoopy bus protocol used to achieve data consistency among the caches and shared memory. (06 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg. 42+8 = 50, will be treated as malpractice.



15CS72

OR

- 8 a. With necessary diagrams, explain the SCI Interconnect models. (06 Marks)
b. Define the following machine parameters to analyze the performance of network. (04 Marks)
c. Explain the following terms:
(i) Data flow graphs. (06 Marks)
(ii) Pure data flow machines. (06 Marks)

Module-5

- 9 a. What are the characteristics of an object oriented programming model? (10 Marks)
b. Explain the functional and logic models in parallel models. (06 Marks)

OR

- 10 a. What is instruction level parallelism? Explain control dependence using code fragment. (10 Marks)
b. Explain the states in 2-bit prediction scheme used for dynamic branch prediction. (06 Marks)

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